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	APPLICABLE DIVISION	
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SPECIFICATION

SPECIFICATION FOR
 Passive **Matrix** COLOR LCD Module

Model No.
LM16X212

CUSTOMER'S APPROVAL

DATE _____

BY _____

PRESENTED BY *Y. Inoue*

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RECORDS OF REVISION

SPEC. No.

LC95408

MODEL No

LM16X212

DOC. FIRST ISSUE

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DATA	SPEC	REVISED	REVISED	REF.	SUMMARY	DATE
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DATE & APPROVAL

1. Overview

The LM16X212, dot-matrix LCD module consists of a 5 X 7-dot 16-character 2-line dot-matrix LCD panel, LCD driver, controller LSI and yellow green backlight LED fabricated on a single PCB. Incorporating mask ROM-based character generator and display data RAM in the controller LSI, the module can efficiently display the desired characters under microprocessor control. LCD is positive type.

(Features)

- (1) The LCD of the module is STHC (Super Twisted High Contrast) yellow green transmissive type.
- (2) Low power consumption with the dot-matrix LCD panel and CMOS LSI. Built-in backlight LED with high luminance and stable radiation.
- (3) Thin, lightweight design permits easy installation in a variety of equipment.
- (4) Allowing for being connected at general-purpose CMOS signal level, the module can be easily interfaced to a microprocessor with common 4-bit and 3-bit parallel inputs and outputs.
- (5) Built-in character generator ROM and RAM, and display data RAM:

Character generator ROM

160 different 5 X 7 dot-matrix character patterns
(Alphanumeric and symbols)

Character generator RAM

8 different user programmed 5 x 7 dot-matrix patterns

Display data RAM

30 X 8 bits

- (6) Numerous instructions
Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF, Blink character, Cursor shift, Display shift
- (7) Built-in reset circuit is triggered at power ON.
(For the operating conditions, refer to the separate user's manual "Dot-Matrix LCD module with built-in controllers".)
- (8) The module operates from a single 5v power supply.

* As to the packing, refer to the separate "COMMON PACKING SPECIFICATION FOR LM16255 series".

2. Construction and Outline

Construction : 5 X 7 dot + cursor, 16-character 2-line dot-matrix display module (Built-in Yellow-green backlight LED, positive type)

Outline : See Fig.7.

Interface signals : See Table 5.

Character pattern details : See Fig.7.

Character codes : See Table 9.

There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function. Rejection criteria shall be noted in Inspection Standard (S-U-009).

3 Mechanical Specifications

Table 1

Parameter	Specification	Unit
Outline dimensions	34(W) X 44(H) X 16 MAX(D)	mm
Effective display area	61(W) X 15.8(H)	mm
Display format	16 characters X 2 lines	-
Character format	5 X 7 dots with cursor	-
Character size	2.96(W) X 4.86(H) (5 X 7 dots)	mm
Dot size	0.56(W) X 0.66(H)	mm
Dot spacing	0.04	mm
Character color *	Dark blue	-
Backlight color	Yellow green	-
Weight	Approx. 40	g

* Due to characteristics of the LC Material, the color vary with environmental temperature

4. Electrical Specifications

4.1 Absolute maximum ratings

Table 2

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply voltage(Logic)	VDD-VSS	-0.3	5.5	V	
Supply voltage(LCD drive)	V0-VSS	0	5.5	V	VDD>V0
Supply current(Backlight LED)	ILED	-	240	mA	Ta=25°C
Input voltage	VIN	-0.3	VDD+0.3	V	
Storage temperature	Tstg	-25	70	°C	
Operating temperature	Topt	0	50	°C	
Reverse voltage(Backlight LED)	VLED-VLSS	-5	-	V	

4.2 Electrical characteristics

Table 3

(Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	
Supply voltage(Logic)	VDD-VSS	4.75	5	5.25	V		
Supply voltage (LCD drive)	V0-VSS		0.65*		V	VDD=5V	
Input voltage	"L"	VIL	-0.3	-	0.5	V	
	"H"	VIH	2.2	-	VDD	V	
Output voltage	"L"	VOL	-	-	0.4	V	IOL=1.2mA
	"H"	VCH	2.4	-	-	V	-IOH=0.205mA
Input leakage current	IIL	-	-	1	µA		
Internal oscillating frequency	fosc		250		KHz		
Supply current	IDD		1.6	2.2	mA	VDD=5V, V0=0V	
	ILED		120	180	mA	VLED-VLSS=5V	
Power dissipation	Pd		603	911	mW	VDD=5V, V0=0V VLED-VLSS=5V	
Supply voltage (Backlight LED)	VLED-VLSS	4.75	5	5.25	V		

* Note. After over 30 minutes since backlight begin lighting.

4.3 Timing characteristics

Table 4

VDD=5.0V±5%
Ta=0~50°C

Parameter	Symbol	Min.	Typ.	Max.	Unit
Enable cycle time	t _{cyceE}	1000	-	-	ns
Enable pulse width	PWEH	450	-	-	ns
Enable rise/fall time	t _{Er} , t _{Ef}	-	-	25	ns
RS, R/W setup time	t _{AS}	140	-	-	ns
Address hold time	t _{AH}	10	-	-	ns
Data setup time	t _{DSW}	195	-	-	ns
Data delay time	t _{DDR}	-	-	320	ns
Data hold time(write)	t _H	10	-	-	ns
Data hold time(read)	t _{DHR}	20	-	-	ns

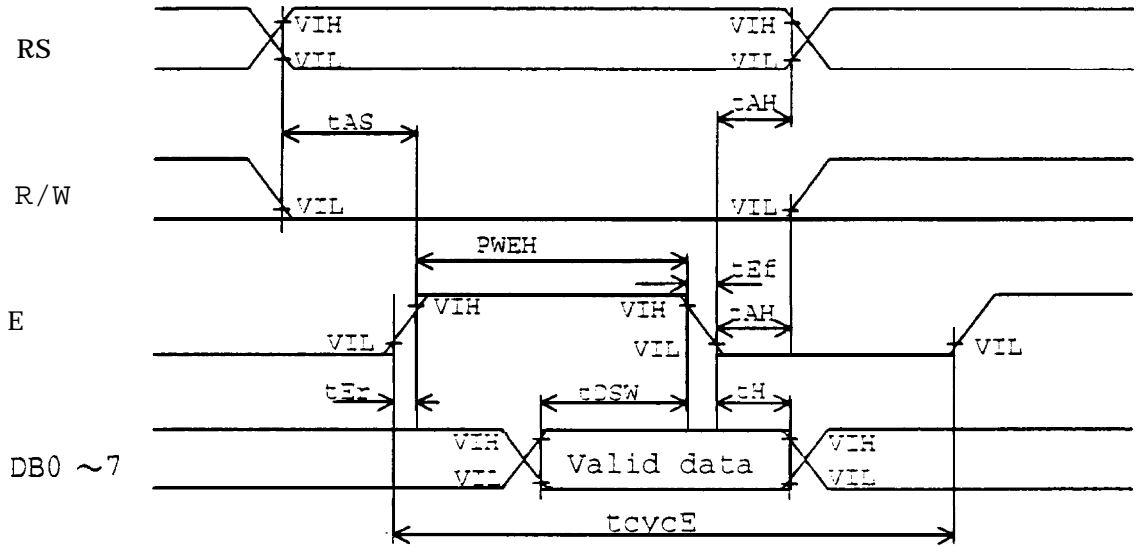
Timing chart: See Fig.1.

4.4 Interface signals

Table 5

Pin No.	Symbol	Description	Connection
1	VSS	Ground potential	GND:0V
2	VDD	Power supply	+5V
3	V0	Contrast adjustment voltage	Adjust the contrast by changing the supply voltage from 0V to 5V.
4	RS	Register select signal	Control signal inputs (For details, see section 6 and 7.)
5	R/W	Read/write select signal	
6	E	Operation(data read/write enable signal)	
7	DB0	Code I/O data LSB	Data bus line :DB7 may also be used to check the busy flag. :Lines DB0~DB3 are not used when interfacing with a 4-bit microprocessor. (For details, see section 6 and 7.)
3	DB1	Code I/O data 2nd bit	
9	DB2	Code I/O data 3rd bit	
10	DB3	Code I/O data 4th bit	
11	DB4	Code I/O data 5th bit	
12	DB5	Code I/O data 5th bit	
13	DB6	Code I/O data 7th bit	
14	DB7	Code I/O data MSB	
15	VLED	Power supply (-)	5V power supply between VLED and VLSS.
16	VLSS	Power supply (-)	

Write Operation



Read Operation

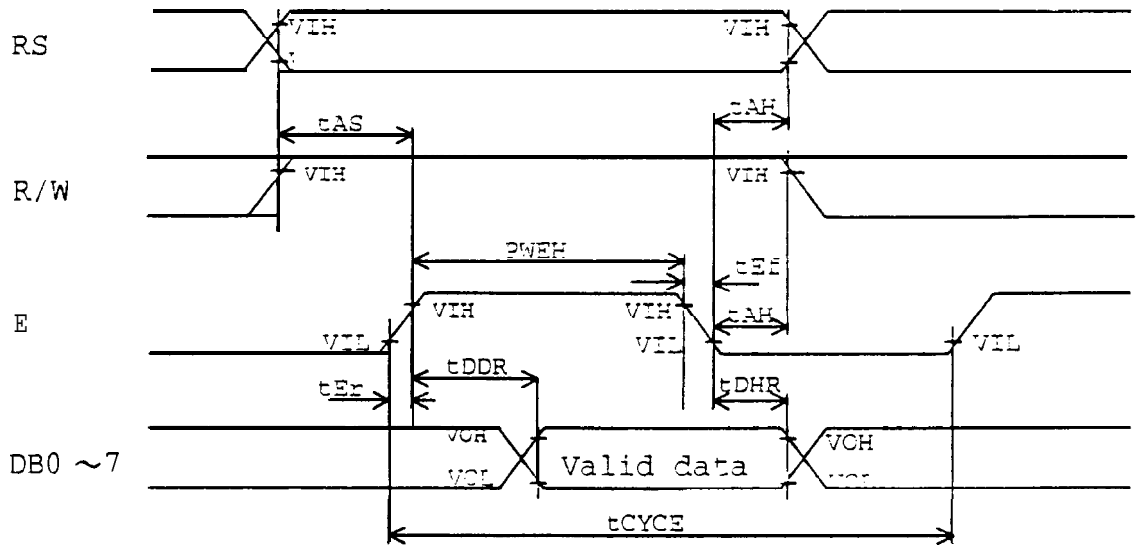


Fig.1 Timing Chart

5. Optical Characteristics

5.1 When backlight LED is OFF state

Table 6 shows the optical characteristics when LCD drive voltage is adjusted to the maximum contrast in $\theta = 0^\circ$.

Table 6

(Ta=25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark		
Viewing angle range	$\theta_2 - \theta_1$	$\phi = 0^\circ$ $\theta_1 < \theta_2$	$C_o \geq 2.0$	60	-	-	dgr.	Note 1	
	θ_1	$\theta_1 < \theta_2$	$C_o = 2.0$	-	-	-25	dgr.	Note 1	
	θ_2			25	-	-			
	Viewing angle range	$\theta_2 - \theta_1$	$\phi = 45^\circ$ 315°	$C_o \geq 2.0$	60	-	-	dgr.	Note 1
		θ_1	$\theta_1 < \theta_2$	$C_o = 2.0$	-	-	-25	dgr.	Note 1
		θ_2			25	-	-		
Contrast ratio	C_o	$\theta = 0^\circ, \phi = 0^\circ$	5	3	-		Note 2		
Response time	Rise	t_r	$\theta = 0^\circ, \phi = 0^\circ$	-	150	250	ms	Note 3	
	Decay	t_d	$\theta = 0^\circ, \phi = 0^\circ$	-	150	250	ms	Note 3	

Note 1) The viewing angle range is defined as shown below.

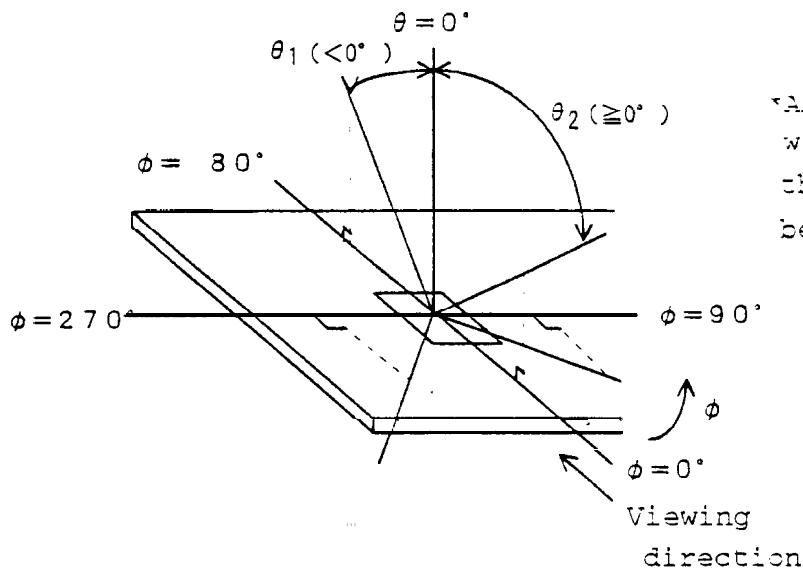


Fig.2 Definition of viewing angle

Note 2) Contrast ratio is defined as follows:

When input signal is applied to the unit to select (turn on) the LCD dots (pixels) to be measured in the optical characteristics test method as defined in Fig.3.

$$\text{Contrast ratio} = \frac{\text{Photodetector output voltage with non-select waveform being applied}}{\text{Photodetector output voltage with select waveform being applied}}$$

Note 3) When input signal for selecting or non-selecting the dots to be measured are applied using the optical characteristics test method shown in Fig.3. The response characteristics of the photo-detector output are measured as shown in Fig.4.

616
KETHLEY
DIGITAL
ELECTRO METER

Contrast
Detector

Response time
Detector

PERKINELMER
TYPE50P
STORAGE
OSCILLOSCOPE

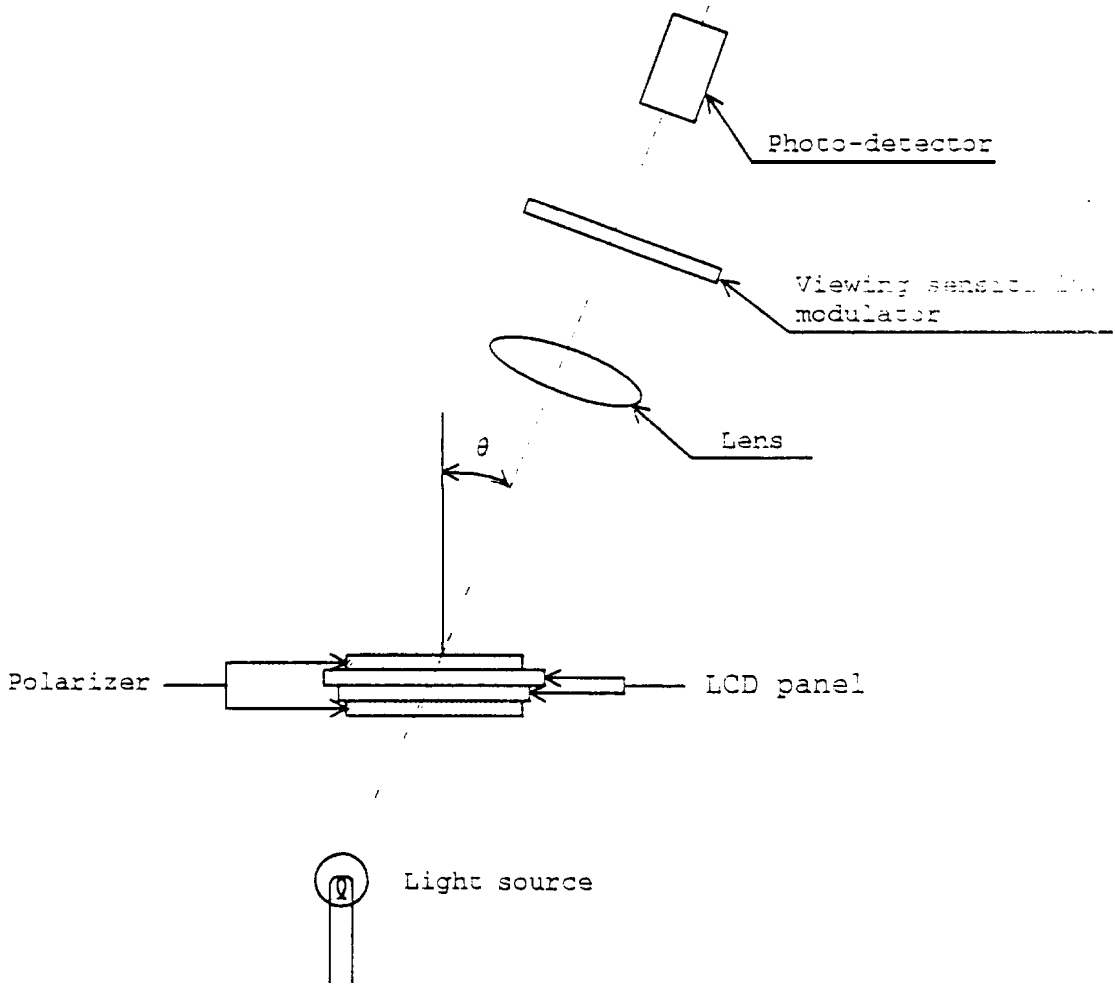


Fig. 3 optical Characteristics Test Method

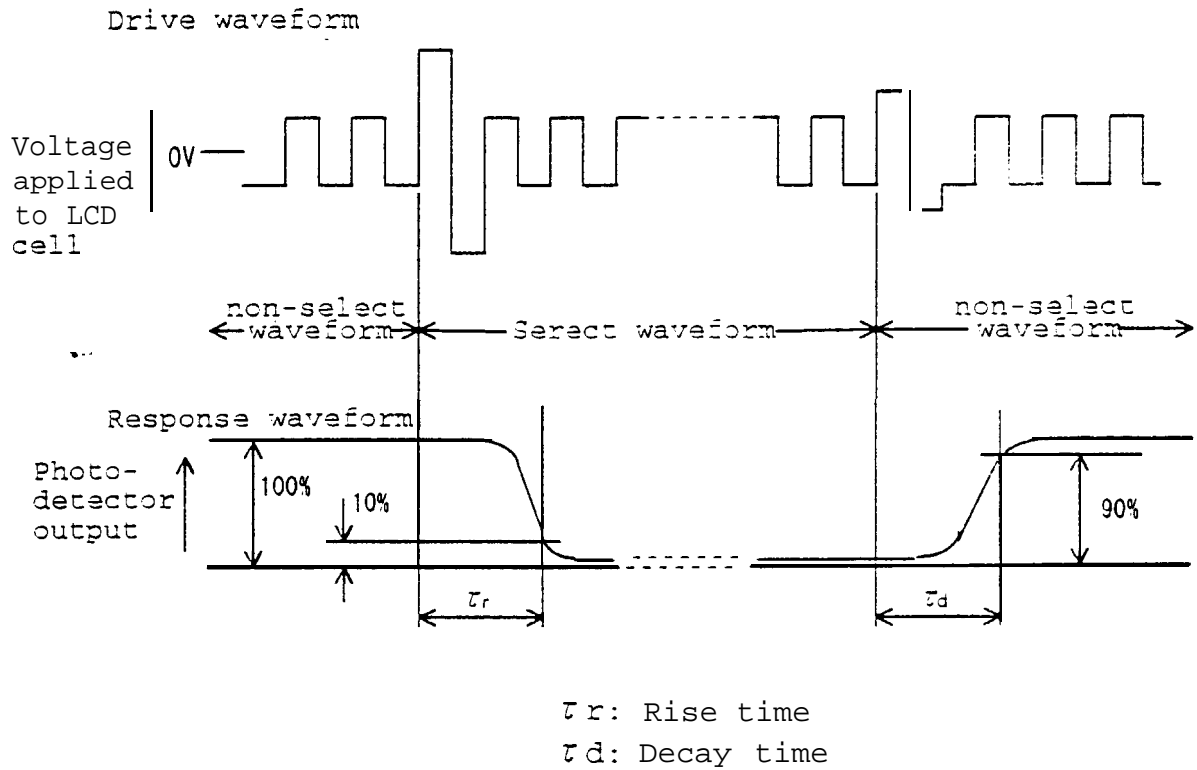


Fig.4 Definition of Response Time

5.2 Characteristics of Backlight LED (When LCD is OFF state)

Table 7

Ta=25°C

VLED-VLSS=5V

Parameter	Min.	Typ.	Max.	Unit	remark
Luminance *		25	-	cd/m ²	
Peak emission wavelength	-	565	-	nm	
Spectrum radiation bandwidth	-	30	-	nm	

* Note. Center of the module with LED backlight lit.

6. Pin Description

1) VDD and VSS Pins

VDD and VSS pins are for power supply. VSS pin is grounded, and VDD pin is supplied with +5V. Each voltage necessary to drive LCD is generated in the module.

2) RS Pin

The controller LSI has two 8-bit registers; an instruction register (IR) and a data register (DR). RS signal selects these registers.

IR stores instruction codes such as display clear, shift, etc. and also stores address information for the display data RAM (DD RAM), character generator RAM (CG RAM);

DR is used for temporarily storing data to be written into DD RAM and CG RAM.

" 0 " :Instruction register (when writing)

" 1 " :Data register (read/write)

3) R/W Pin

Read or write select signal Pin.

" 0 " :Writing

" 1 " :Reading

4) E Pin

Data read or write operation enable signal pin.

5) DB0~DB7 Pins

Data bus with three-state, bidirectional function for use in data transactions with MPU. DB7 may also be used to check the busy flag.

DB0~DB3 are not used when interfacing with a 4-bit microprocessor.

6) Vo Pin

Viewing angle is varied and contrast is adjusted 'by changing voltage between +5V~0V by applying bias voltage to the LCD driver.

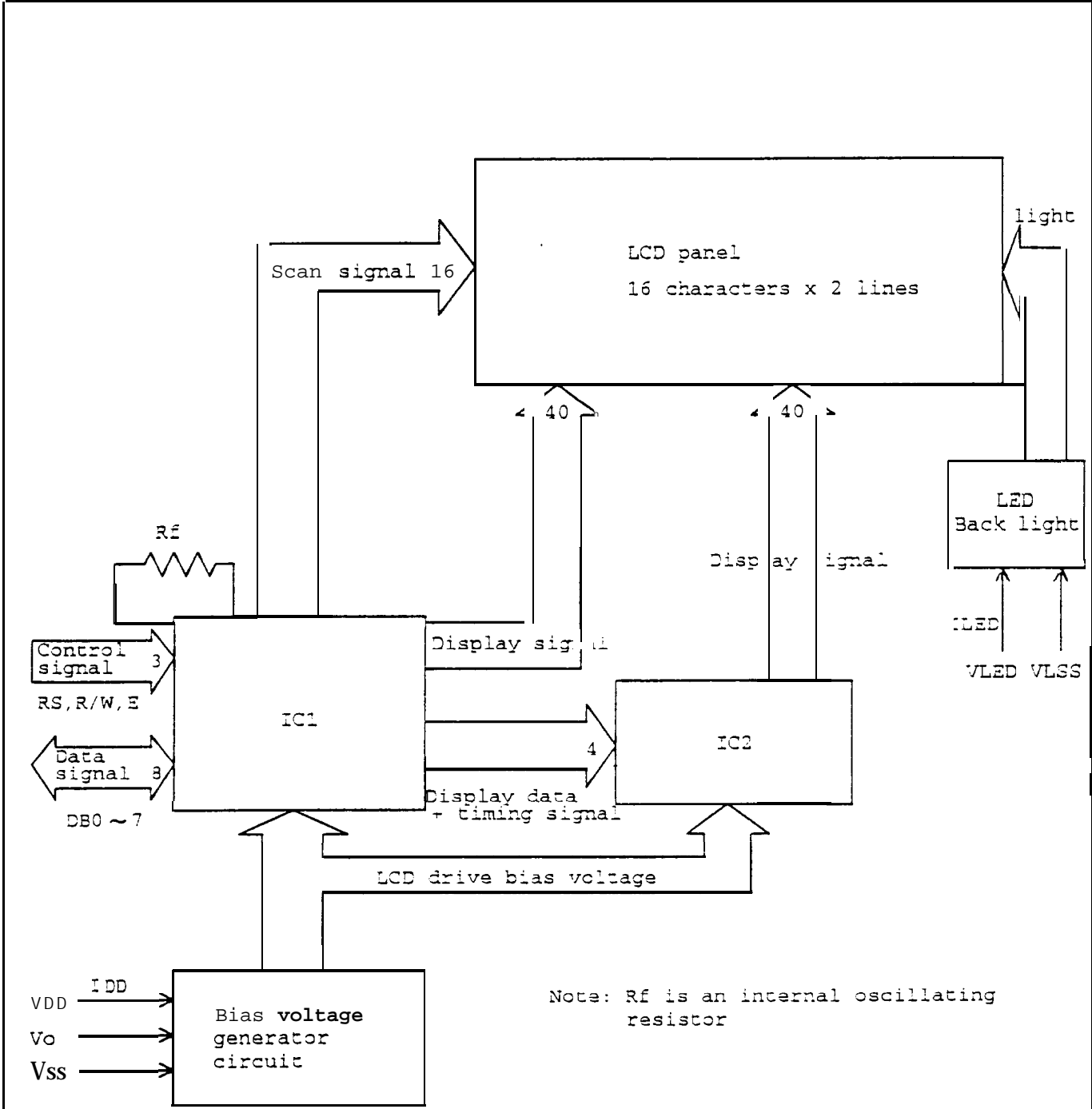
7) VLED and VLSS

Power supply for LED backlight. (By changing the supply voltage, backlight luminance can be adjusted.)

VLED is plus and VLSS is minus.

Instruction	C o l e										Function
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Display clear	0	0	0	0	0	0	0	0	0	1	Clear entire display area, restore display from shift, and load address counter with DD RAM address 00H.
Display/ cursor home	0	0	0	0	0	0	0	0	1	*	Restore display from shift and load address counter with DD RAM address 00H.
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Specify cursor advance direction and display shift mode. This operation takes place after each data transfer.
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Specify activation of display (D), cursor(C), and blinking of character at cursor position(B).
Display/ cursor shift	0	0	0	0	0	1	S/C	R/L	*	*	Shift display or move cursor.
Function set	0	0	0	0	1	DL	1	0	*	*	Set interface data length(DL)
CG RAM address set	0	0	0	1	ACG					Load the address counter with a CG RAM address. Subsequent data is CG RAM data.	
DD RAM address set	0	0	1	ADD					Load the address counter with a CG RAM address. Subsequent data is DD RAM data.		
Busy flag/address counter read	0	1	BF	AC					Read busy flag(BF) and contents of address counter(AC).		
CG RAM/DD RAM data write	1	0	Write data					Write data to CG RAM or DD RAM.			
CG RAM/DD RAM data read	1	1	Read data					Read data from CG RAM or DD RAM.			

/D=1: Increment	I/D=0 Decrement	S/C=1: Shift display	S/C=0 Move cursor
=1: Shift display	S =0 Freeze display	R/L=1: Shift right	R/L=0 Shift left
=1: Display ON	D =0 Display OFF	DL=1: 8-bit	DL =0 4-bit
=1: Cursor ON	C =0 Cursor OFF	BF=1: During internal operation	BF =0 End of internal operation
=1: Character at cursor position blinks	B =0 Character at cursor position unblinks.		



Note: Rf is an internal oscillating resistor

Fig. 5 Block Diagram

IC1 : K50066F00 (SAMSUNG)
 IC2 : MSM5254 (OKI)

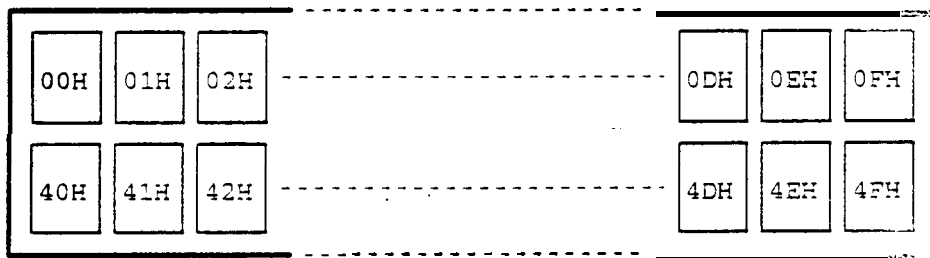


Fig.6 Display Address (When the display is not shifted)

Table 9 InputCode vs. Character Pattern

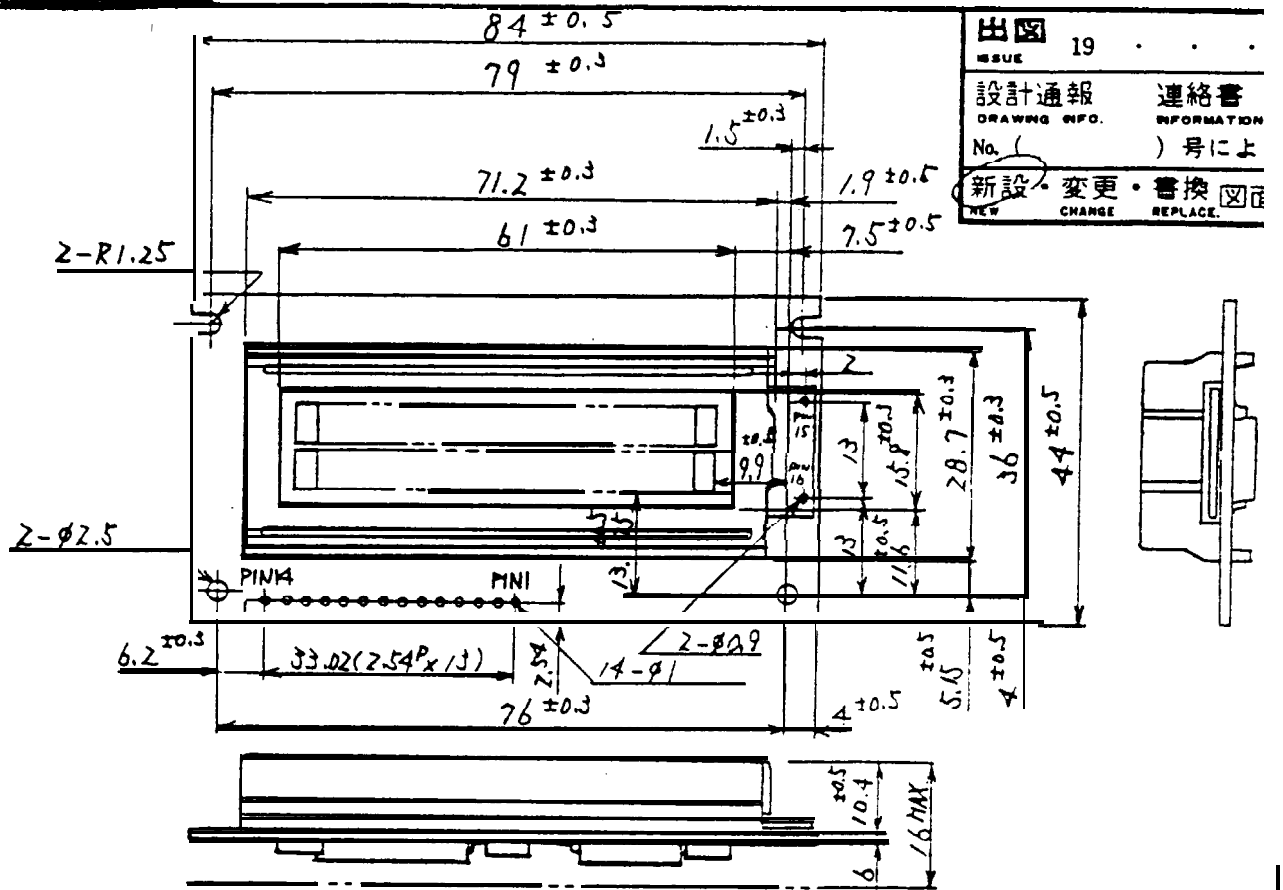
*1 *2 4bit 4bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)												*
xxxx0001	(2)												
xxxx0010	(3)												*
xxxx0011	(4)												
xxxx0100	(5)												*
xxxx0101	(6)												
xxxx0110	(7)												*
xxxx0111	(8)												*
xxxx1000	(1)												
xxxx1001	(2)												*
xxxx1010	(3)												*
xxxx1011	(4)												
xxxx1100	(5)												
xxxx1101	(6)												
xxxx1110	(7)												
xxxx1111	(8)												*

Note 1. CG RAM is character generator RAM in which user-defined patterns are stored.

Note 2. X mark: prohibition of input

*1 High-order, *2 Low-order

SHARP



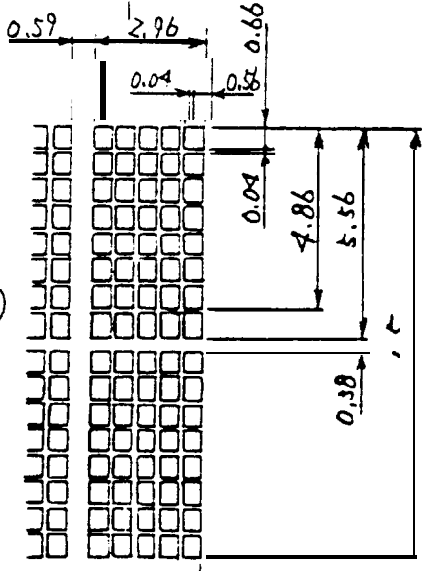
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設計通報 **連絡書**
 DRAWING INFO. INFORMATION
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新設 **変更** **書換** **図**
 NEW CHANGE REPLACE.

*	**
1	V _{SS}
2	V _{DD}
3	V ₀
4	RS
5	R/W
6	E
7	DB ₀
8	DB ₁
9	DB ₂
10	DB ₃
11	DB ₄
12	DB ₅
13	DB ₆
14	DB ₇

* Pin No.
 ** Display Signal

Dot Size
 (φ = 5/1)

*	**
15	V _{LED}
16	V _{SS}



指示なき寸法公差は とする
 UNSPECIFIED TOL TO BE

19 . . .				LM16X21Z	指示なき寸法公差は とする
19 . . .				LM16X21A	UNSPECIFIED TOL TO BE
年月日	訂正記事	投通No.	担当	適用機種	名 称
DATE	REVISE	PREPA		MODEL	Fig. 7 Unit Outline Dimensions
材 質	板厚	仕 上	尺 度		記 号
MATERIAL	THICKNESS	FINISH	SCALE		部 品 コード
					PARTS CODE
計 画	検 査	検 査	承認		
TRACER	CHECK	CHECK	APPROVE	SHARP CORPORATION	
				発行部門 LCD Division	
				作成日付	19 86 . 9 . 4 .
				図 番	0 D 1 6 2 1 A 0 1 1 0 1 1
				DRAWING No.	